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Declaration
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of : Yushi INOUE
Serial No. : 09/826,833
Filed : April 6, 2001
For : Method for Producing Semiconductor Device

DECLARATION

I, Masami ONO, declare that I am acquainted with both the Japanese and English languages, that the English translation attached hereto is a true and accurate translation of Japanese Patent Application No. 2000-124324.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Signed at Osaka, Japan on this 3rd day of July, 2003

Masami Ono

Masami ONO

PATENT OFFICE
JAPANESE GOVERNMENT

This is to certify that the annexed is a true copy of the following application as filed with this office.

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Application Number: Patent Application No. 2000-124324

Applicant(s): SHARP KABUSHIKI KAISHA

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[TITLE OF THE INVENTION] Method for Producing Semiconductor Device

[CLAIMS]

[Claim 1] A method for producing a semiconductor device comprising;

forming an opening by etching using a resist pattern in a multi-layered film having a first organic insulating film, a first etching stop film and a second organic insulating film layered in this order such that the opening penetrates from the second organic insulating film to the first organic insulating film,

wherein a second etching stop film is formed between the resist pattern and the second organic insulating film to protect the second organic insulating film from being etched during the formation of the opening.

[Claim 2] A method for producing a semiconductor device as claimed in Claim 1, wherein the first etching stop film and the second etching stop film are made from the same material.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Industrially Applicable Field]

The present invention relates to a method for producing a semiconductor device, and more detail, it relates to a method for producing a semiconductor device having a multi-layered interconnection structure comprising an organic insulating film, particularly an organic insulating film having a low dielectric constant

by means of dual damascene process.

[0002]

[Prior Art and Problems that the Invention is to solve]

Recently, as semiconductor devices become finer and more multi-layered, interconnection delay has become a serious problem.

In other words, finer transistors have been implemented thus far in accordance with the scaling law for realizing higher device operation performance. On the other hand, however, finer interconnections have increased the interconnection resistance and the interconnection capacitance, and the interconnection delay expressed by RC is no longer negligible with respect to the operation speed of LSI.

[0003]

Finer interconnections have also increased the current density in the interconnection, and lower reliability of the interconnection ascribed to the electromigration as well as an increase in power consumption due to the increase in interconnection capacity is also a severe problem.

In order to overcome the aforementioned problems, Cu is being used as the interconnection material because it has a lower resistance and a higher electromigration resistance than Al. However, since Cu is difficult to be processed by a conventional dry etching technique, damascene process using CMP technique is widely studied. In particular, a dual damascene process which forms the interconnection and a buried plug of the connection holes at the same time has been recently developed.

[0004]

For instance, in the unexamined published Japanese patent application Hei 11(1999)-186391, a method for producing a semiconductor by a dual damascene process such as following is proposed.

Firstly, as shown in Fig. 2(a), a first etching stop film 31, a second interlayer insulating film 22, a second etching stop film 32, and a third interlayer insulating film 23 are sequentially formed in this order on a first interlayer insulating film 21 having a first metallic interconnection 14 partially buried therein.

[0005]

Subsequently, as shown in Fig. 2(b), a resist pattern 15 for forming a via hole is formed on the third interlayer insulating film 23, and the second etching stop film 32 and the third interlayer insulating film 23 are etched using the resist pattern 15 as a mask, under etching conditions such that the etching rate may be the same for the second etching stop film 32 and the third interlayer insulating film 23. At the point etching reaches the second interlayer insulating film 22, the second interlayer insulating film 22 is etched using the resist pattern 15 as a mask again under the etching conditions such that the etching rate of the etching stop film 31 is sufficiently lower than that of the second interlayer insulating film 22.

[0006]

Then, as shown in Fig. 2(c), the first etching stop film 31 under the second interlayer insulating film 22 is removed by etching,

still using the resist pattern 15 as a mask, by changing the etching conditions. A via hole 16 can be formed in this manner.

[0007]

After stripping off the resist pattern 15, as shown in Fig. 2(d), a resist pattern 17 for forming an interconnection groove is formed on the third interlayer insulating film 23, and the third interlayer insulating film 23 is etched using this resist pattern 17 as a mask under the etching conditions such that the etching rate of the second etching stop film 32 is sufficiently lower than that of the third interlayer insulating film 23. Thus is formed an interconnection groove 18 connected to the first metallic interconnection 14 through the via hole 16.

[0008]

Subsequently, a metallic film is formed on the entire surface so that the via hole 16 and the interconnection groove 18 are completely buried. Then, as shown in Fig. 2(e), the metallic film that is provided on the third interlayer insulating film 23 is removed by CMP process to form the metallic interconnection and the connecting plug 19 monolithically inside the interconnection groove 18 and the via hole 16, respectively.

In the above-mentioned process, however, the via hole 16 is opened after forming the resist patterns 15 and 17 directly on the third interlayer insulating film 23. Thus, in case an organic insulating film having a low dielectric constant, which is frequently used in recent years to reduce the interconnection capacity, is used for the third

interlayer insulating film 23, there occurs a problem that the organic insulating film is also etched when opening the via hole.

[0009]

In other words, in the case where a via hole is formed through two or more layers of organic insulating film, i.e., through the third and the second interlayer insulating films in the dual damascene process as described above, the resist pattern also is gradually etched during the same time because the etching rate of the organic insulating film is approximately the same as that of the resist, and the resist pattern suffers thinning gradually as to expose the surface of the third interlayer insulating film. This leads to a problem of causing etching of the third interlayer insulating film before the completion of forming the via hole.

[0010]

In order to prevent the aforementioned problem from occurring, the thickness of the resist pattern needs to be thicker than at least the total thickness of the second interlayer insulating film 22 and the third interlayer insulating film 23. However, if the thickness of the resist pattern is too thick, an abnormal pattern formation occurs at the exposure as to cause an another problem that patterning can not be performed completely to provide a predetermined shape (e.g., in the case of patterning 0.12 μm wide patterns, the upper limit of the thickness of the resist is about 500 nm).

In the unexamined published Japanese patent application Hei 10(1998) -112503, the following technique is proposed.

[0011]

Firstly, as shown in Fig. 3(a), a silicon oxide film 41, an organic film 42 having a low dielectric constant, a silicon oxide film 43 and a resist pattern 44 for forming the interconnection pattern are formed in this order on a silicon substrate 40.

Then, as shown in Fig. 3(b), an opening 45 having a shape corresponding to an interconnection pattern is formed by etching the silicon oxide film by means of dry etching using the resist pattern 44 as a mask. The resist pattern 44 is removed thereafter.

[0012]

Next, as shown in Fig. 3(c), a resist pattern 46 for forming via holes is formed on the silicon oxide film 43 and the organic film 42 having a low dielectric constant by means of photolithography and etching technique.

Then, as shown in Fig. 3(d), the organic film 42 having a low dielectric constant and the silicon oxide film 41 below the opening 45 of the silicon oxide film 43 are selectively and sequentially etched by means of dry etching using the resist pattern 46 as a mask, to form a via hole 47. The resist pattern 46 is removed thereafter.

[0013]

After that, as shown in Fig. 3(e), an interconnection groove 48 is formed by etching the organic film 42 having a low dielectric constant using the silicon oxide film 43 as a mask, and as shown in Fig, 3(f), interconnection material is buried in the via hole 47 and the interconnection groove 48 as to form an interconnection 49.

According to the process above, though the via hole 47 is formed by etching using the resist pattern 46 as a mask, there is no problem of suffering film thinning and a complete removal of the resist pattern during opening of a via hole since the organic film having a low dielectric constant is formed as a single layer.

[0014]

However, to suppress an increase in the interconnection capacity of the resulting semiconductor device, it is desired to use an organic insulating film having a low dielectric constant instead of a silicon oxide film. On the other hand, if an organic film having a low dielectric constant is used in place of the silicon oxide film 41, the total thickness of the two layers of organic films having a low dielectric constant exceeds the total thickness of the resist pattern 46. Thus, as in the case described above, there occurs a problem that the surface of the organic film 42 having a low dielectric constant suffers etching.

[0015]

The present invention has been made in view of the aforementioned problems, and its object is to provide a method for producing a semiconductor device which is capable of forming a via hole and an interconnection groove without generating film thinning of the interlayer insulating film provided below an resist pattern even in the case there occurs a thinning of the resist pattern used as a mask when an organic insulating film is applied in a dual damascene process.

[0016]

[Means of solving the Problems]

According to the present invention, it provides a method for producing a semiconductor device comprising;

forming an opening by etching using a resist pattern in a multi-layered film having a first organic insulating film, a first etching stop film and a second organic insulating film layered in this order such that the opening penetrates from the second organic insulating film to the first organic insulating film,

wherein a second etching stop film is formed between the resist pattern and the second organic insulating film to protect the second organic insulating film from being etched during the formation of the opening.

[0017]

[Mode for Carrying out the Invention]

The method for producing a semiconductor device according to the present invention is mainly a method for forming an opening such as a connection hole, an interconnection groove, etc., by means of dual damascene process when forming a multi-layered interconnection structure comprising a multi-layered film constituted of a first organic insulating film, a first etching stop film and a second organic insulating layered in this order.

[0018]

In the method for producing a semiconductor device according to the present invention, the multi-layered film is preferably formed on a semiconductor substrate. As a semiconductor substrate,

materials used in forming a semiconductor device, for example, an elementary semiconductor such as silicon, germanium, etc., and a compound semiconductor such as GaAs, InGaAs, ZnSe, etc., can be mentioned. Among them silicon may be preferred. Furthermore, the semiconductor substrate may be a so-called SOI structure substrate or a multi-layered SOI structure substrate. Still more, the semiconductor substrate may be formed independently or an optional combination with an element isolation film, semiconductor elements such as transistors, capacitors, resistors, etc., a circuit, an insulating film, an interconnection layer, a dummy interconnection layer, etc., below the multi-layered film or in any other region. For instance, electrodes of a transistor and a capacitor or an interconnection layer connected to the electrodes serving as a lower interconnection are formed on a semiconductor substrate, and a first organic insulating film may be formed thereon via an etching stop film. In the case of providing an etching stop film under the first organic insulating film, it is preferred that the etching stop film is an insulating film which functions diversely, for example, as a diffusion barrier for metallic elements and impurities such as copper, phosphorus, arsenic, boron, etc. Specifically, silicon nitride films, silicon carbide films, etc., are mentioned.

[0019]

As the first organic insulating film constituting the lowermost layer of the multi-layered film, any type of film is used as long as it is an insulating film constituted of an organic material. For example, a

single layer or a multi-layered film of polytetrafluoroethylene, fluorinated polyallyl ether, fluorinated polyimide, etc., can be mentioned. Also, those having a dielectric constant of about 3 or lower can be mentioned. Particularly preferred among them are those having a low dielectric constant, such as those having a dielectric constant of about 1.8 or lower. As specific examples of the first organic insulating film, single layered film or multi-layered films of FLARE (trade name, Allied Signal Inc.), SiLK (trade name, The Dow Chemical Company), etc., can be mentioned. The film thickness of the first organic insulating film may be properly adjusted depending on the material, the film thickness, etc., of the second organic insulating film and the first etching stop film which are described hereinafter, or on the function of the targeted semiconductor device. For instance, the film thickness is preferably set to a thickness corresponding to the height of the connection holes such as those denoted as via holes, contact holes, through holes, etc., as with the film thickness of the first etching stop film described hereinafter. More specifically, the thickness of the first organic insulating film may be about 50 to 100 nm.

[0020]

There is no particular limitations to the first etching stop film formed on the first organic insulating film, as long as it functions as an etching stopper when etching is performed to the second organic insulating film formed on the first etching stop film described hereinafter under the selected etching process and conditions

described hereinafter. However, the etching stop film preferably is an insulating film. The term "functions as an etching stopper" as referred herein signifies that the selectivity ratio with respect to the second organic insulating film (etching rate of the second organic insulating film/etching rate of the first etching stop film) is high. The selectivity ratio can be properly adjusted depending on the material, etc., of the second organic insulating film. For example, a value of about 5 or higher, or about 10 or higher, preferably about 15 or higher, and more preferably about 20 or higher can be mentioned.

[0021]

As material of the first etching stop film, for example, a single layer or a multi-layered films of silicon oxide, silicon nitride, BPSG, PSG, BSG, AsSG, etc., can be mentioned. Particularly preferred among them is a silicon oxide film. The film thickness of the first etching stop film is not particularly limited, but a thickness of about 50 to 100 nm can be mentioned as an example. In the case of using a silicon oxide film, in particular, a film can be formed stably at a thickness of about 50 nm, but when the film is provided thicker than those having a film thickness of about 100 nm, the resulting semiconductor device may suffer a large interconnection capacity attributed to the relatively high dielectric constant.

[0022]

The second organic insulating film that is formed on the first etching stop film may be made of material properly selected from those mentioned for the first organic insulating film. Particularly preferred

is to use the same material as that used in the first organic insulating film. The film thickness of the second organic insulating film may be properly adjusted depending on the material, the film thickness, of the first organic insulating film and the first etching stop film, etc., or on the function and the like of the targeted semiconductor device. For example, it is preferable that the film thickness for the second organic insulating film corresponds to the film thickness of a general interconnection layer. Specifically, the film thickness of the second organic insulating film may be about 300 to 1,000 nm.

[0023]

Material used for the resist pattern is not particularly limited as long as it comprises a resist used in an ordinary photolithography process, and both positive type and negative type resists can be used. For instance, a novolak-naphthoquinonediazide based resist, a cyclized rubber-bisazide based resist, a chemically sensitized resist, etc., can be mentioned. Since the resist pattern is used as a mask on etching the first etching stop film, the second etching stop film, the first organic insulating film and/or the second organic insulating film, the selectivity ratio with respect to these films (etching rate of the resist pattern/etching rate of these films) needs to be small. Although the selectivity ratio differs depending on the material constituting the resist pattern, the materials constituting these films, the etching method and conditions, etc., it is preferable to have a value of less than 1.

[0024]

As the shape of the resist pattern, a variety of shapes such as

those having the connection holes such as so-called via holes, contact holes, through holes, etc., or those having the opening corresponding to the interconnection and the like can be mentioned.

As the film thickness of the resist pattern, there is no particular limitation as long as it is capable of forming a proper pattern shape by means of an ordinary photolithography and etching process. For example, in order to form a pattern having a width of an interconnection (e.g., a 0.12 μm width) of the dual damascene process, the film thickness of about 500 nm or less, more specifically, the film thickness of about 200 to 500 nm is suitable.

[0025]

When forming a plurality of openings differing in shape according to the method of the present invention, a plurality of resist patterns may be used. For instance, when forming a connection hole penetrating the first and the second organic insulating films and the first and the second etching stop films, a resist pattern having an opening corresponding to the connection hole is formed at first, and then, when forming an interconnection groove on the second organic insulating film and the second etching stop film, a resist pattern having an opening corresponding to the interconnection groove may be formed. The resist patterns for the connection holes or the interconnection grooves may be formed in a reverse order of the above.

[0026]

The second etching stop film that is formed between the resist pattern and the second organic insulating film needs to be

formed of such a material in such a film thickness that the second organic insulating film is protected from being etched when an opening is formed through the second organic insulating film to the first organic insulating film by etching using the resist pattern.

[0027]

Further, since an opening needs to be formed on the second etching stop film using the above-mentioned resist pattern as a mask, it is preferred that the selectivity ratio with respect to the resist pattern (etching rate of the second etching stop film/etching rate of the resist pattern) is high when etching is performed under proper etching process and etching conditions.

[0028]

As a proper etching process, wet etching using an acid or an alkaline solution, or a mixed solution thereof; and dry etching such as vapor phase etching, plasma etching, RIE, sputter etching, ion beam etching, photoetching, etc., can be mentioned, and particularly preferred among them are vapor phase etching, plasma etching, etc.

[0029]

In the case of performing wet etching, the etching conditions refer to a type of a solution used, temperature, a method of contacting the solution, contact duration, etc. In the case of dry etching, the etching conditions refer to a type of an etching apparatus, a type or an combination of gases used as an etchant, a flow rate, power, pressure, etc.

A high selectivity ratio signifies, for example, a value of about

5 or higher, or about 10 or higher, preferably about 15 or higher, and more preferably, about 20 or higher.

[0030]

As material for the second etching stop film, for instance, those properly selected from the materials mentioned above for the first etching stop film can be used. Among them, particularly preferred is to select the same material used for the first etching stop film, because it is advantages in that an apparatus for depositing the first etching stop film can be utilized as it is, and that the etching selectivity ratio of the first etching stop film can be applied as it is. The film thickness of the second etching stop film may be properly adjusted depending on material, film thickness, etc., of the first and the second organic insulating films and the first etching stop film, or on the function and the like of the targeted semiconductor device. However, it is preferred that the film thickness of the second etching stop film is thicker than that of the first etching stop film. Specifically, the film thickness of the second etching stop film may be about 250 to 500 nm.

Embodiments of the method for producing a semiconductor device according the present invention are described below with reference to the attached drawings.

[0031]

Firstly, as shown in Fig. 1(a), an etching stop film of about 10 to 100 nm in film thickness, for example, a silicon nitride film 2 of about 50 nm; a FLARE film of about 500 nm as a first organic polymer insulating film 3; a silicon oxide film of about 100 nm as a first etching

stop film 4; a FLARE film of about 500 nm as a second organic polymer insulating film 5; a silicon oxide film of about 300 nm as a second etching stop film 6; and a resist pattern 7 of about 500 nm for forming a via hole are formed in this order on a lower interconnection layer 1. The silicon nitride film 2 also functions as a diffusion barrier film for Cu on the lower interconnection layer 1.

[0032]

Then, as shown in Fig. 1(b), the second etching stop film 6 is etched by using the resist pattern 7 as a mask. Here, the etching is performed under the following conditions:

Gas flow rates: C_4F_8 10 to 15 sccm,

CO 80 to 100 sccm,

O_2 2 to 5 sccm,

Ar 50 to 70 sccm,

Power: 1,500 to 1,700 W; and

Pressure: 50 to 60 mTorr.

The selectivity ratio (the second etching stop film 6/the resist pattern 7) in this case is found to be 3.

[0033]

Subsequently, the second organic polymer insulating film 5 is etched using the resist pattern 7 as a mask under the etching conditions such that the first etching stop film 4 is hardly etched as compared with the second organic polymer insulating film 5. Here, the etching is performed under the following conditions:

Gas flow rates: CH_3F 30 to 40 sccm,

O_2 35 to 45 sccm,

N_2 15 to 25 sccm,

Power: 400 to 500 W; and

Pressure: 40 to 50 mTorr.

In this case, as is shown in Fig. 1(c), the resist pattern 7 is gradually etched, with a selectivity ratio of the second organic polymer insulating film 5/the resist pattern 7 being 0.8, along with the etching of the second organic polymer insulating film 5. The selectivity ratio of the second organic polymer insulating film 5/the first etching stop film 4 is 20, and etching is almost completely stopped at the first etching stop film 4.

[0034]

Then, as shown in Fig. 1(d), the first etching stop film 4 is etched using the second etching stop film 6 as a mask. The etching conditions used in this step are similar to those employed in the step shown in Fig. 1(b). In this etching, the second etching stop film 6 is etched together with the first etching stop film 4. Thus, the second etching stop film 6 undergoes thinning, but is not completely removed.

[0035]

After that, as shown in Fig. 1(e), the first organic polymer insulating film 3 is etched using the second etching stop film 6 as a mask under the conditions such that the etching stop film 2 is hardly etched compared to the first organic polymer insulating film 3. The etching conditions used in this step are similar to those employed in the step shown in Fig. 1(c). The etching can be stopped almost

completely at the etching stop film 2. The connection hole 8 is formed in this manner.

Then, as is shown in Fig. 1(f), a resist pattern 9 for forming the interconnection groove is formed on the second etching stop film 6 at a film thickness of about 500 nm.

[0036]

Next, as shown in Fig. 1(g), the second etching stop film 6 is etched using the resist pattern 9 as a mask under the etching conditions such that the etching rate of the etching stop film 2 is sufficiently slower than that of the second etching stop film 6.

Sequentially, the second organic polymer insulating film 5 is etched using the resist pattern 9 as a mask under the etching conditions such that the first etching stop film 4 and the etching stop film 2 are hardly etched compared to the second organic polymer insulating film 5. The etching conditions used in this step are similar to those employed in the step shown in Fig. 1(c). In this etching step, as is shown in Fig. 1(h), the resist pattern 9 is gradually etched together with the etching of the second organic polymer insulating film 5, but the etching can be stopped at the first and the second etching stop films 4 and 6 and the lower interconnection layer 1 of the connection hole 8 is not exposed. The interconnection groove 10 is formed in this manner.

[0037]

Next, as shown in Fig. 1(i), the etching stop film 2 is etched using the second and the first etching stop films 6 and 4 as masks to

thereby expose the lower interconnection layer 1 under the connection hole 8. The etching is performed under the following conditions:

Gas flow rates: CH_3F 5 to 10 sccm,

O_2 45 to 55 sccm,

Power: 200 to 300 W; and

Pressure: 40 to 50 mTorr.

Then, a metallic film is formed in such a manner that the inside of the connection hole 8 and the interconnection groove 10 are completely buried, and as is shown in Fig. 1(j), the metallic film that is present on the second etching stop film 6 is removed by means of CMP method to form an interconnection 11. At this time, the second etching stop film 6 also functions as an etching stopper on removing the metallic film. The second etching stop film 6 is removed for about 100 nm by the CMP process.

[0038]

[Effect of the Invention]

According to the present invention, a second etching stop film capable of protecting the second organic insulating film from being etched during the formation of the opening is formed between the resist pattern and the second organic insulating film. Hence, in the case where a organic insulating film is applied in a dual damascene process, even if the resist pattern suffers thinning during etching or complete removal by etching, the surface of the second organic insulating film can be prevented from being etched by simply forming a second etching stop film.

[0039]

Thus, when forming a plurality of openings differing in shape such as connection holes and interconnection grooves, these openings can be formed continuously by forming a resist pattern corresponding to such openings only once. Hence, the production process can be simplified and the production cost can be reduced. At the same time, the interconnection capacity can be reduced and the insulating film does not suffer thinning so as to produce a semiconductor device of high reliability.

In particular, if the materials of the first and second etching stop films are the same, a film deposition apparatus can be used in common for the formation of stop films, and this enables further reduction of the production cost.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[FIG. 1] Sectional views showing production steps of the essential portions provided for explaining an embodiment of a production method of a semiconductor device according to the present invention;

[FIG. 2] Schematic sectional schedule drawings of the essential portions of a semiconductor device provided for explaining a conventional dual damascene process; and

[FIG. 3] Schematic sectional schedule drawings of the essential portions of a semiconductor device provided for explaining another conventional dual damascene process.

[Explanation of reference numerals]

1 a lower interconnection layer

2 an etching stop film

3 a first organic polymer insulating film (first organic insulating film)

4 a first etching stop film

5 a second organic polymer insulating film (second organic insulating film)

6 a second etching stop film

7, 9 resist patterns

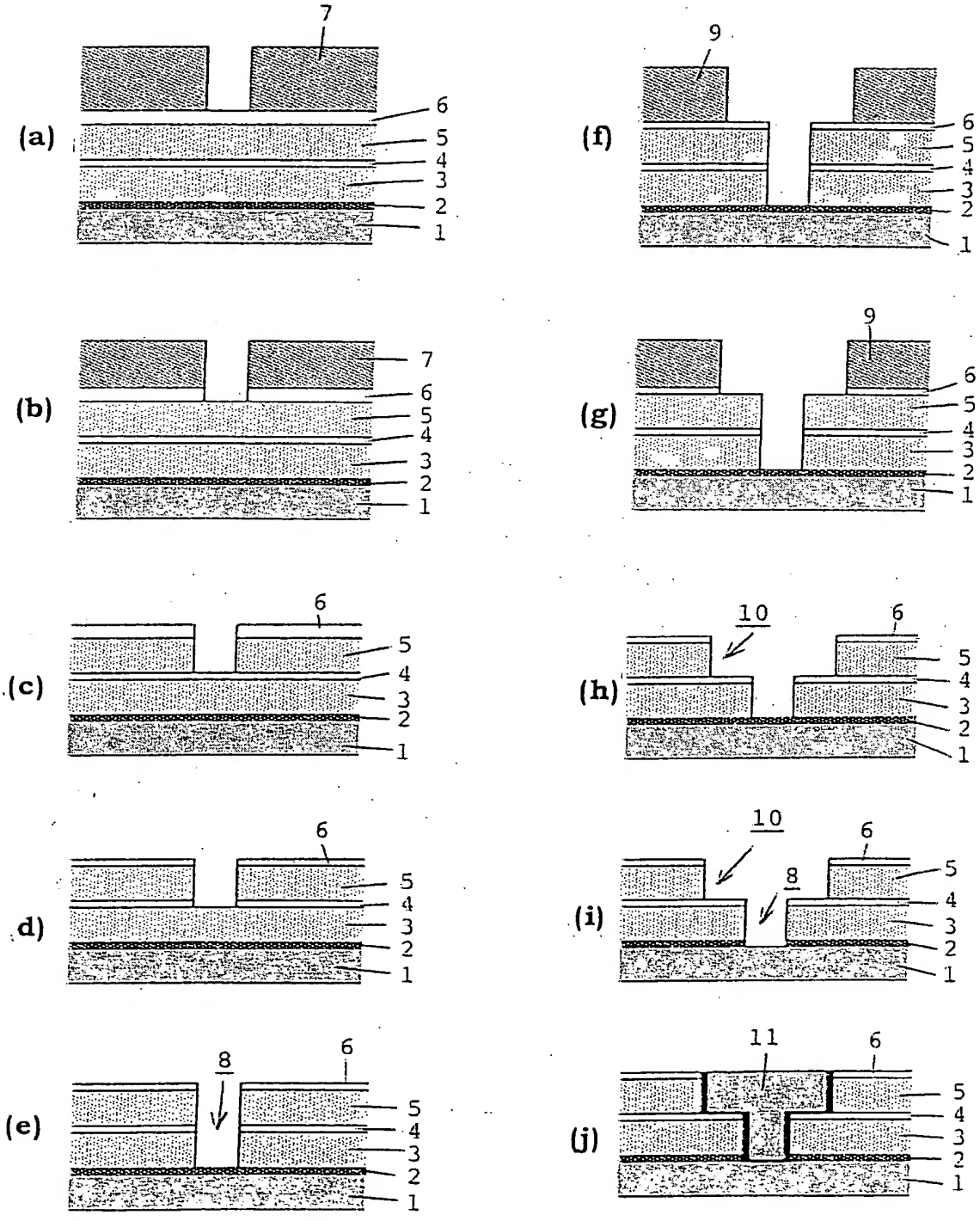
8 a connection hole

10 an interconnection groove

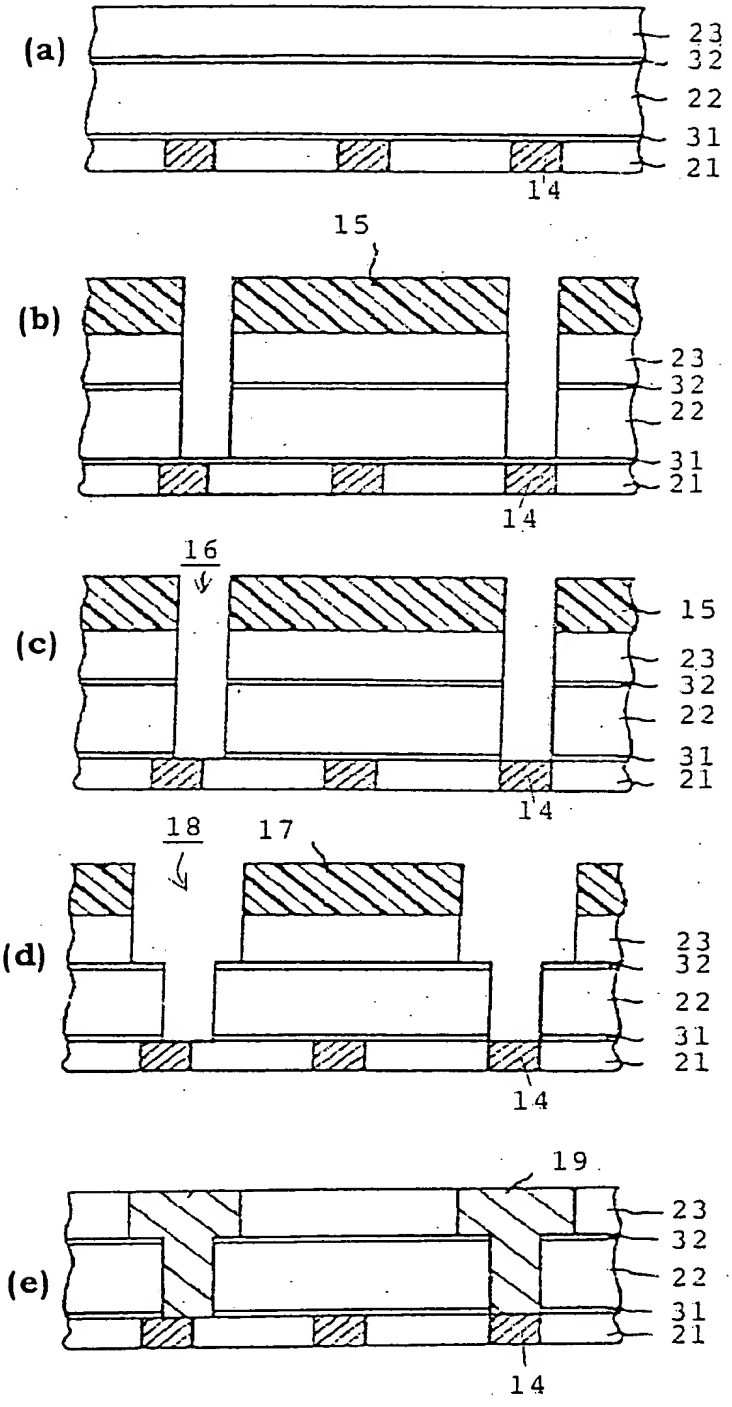
11 an interconnection

[NAME OF THE DOCUMENT] Drawing

[Fig. 1]



[Fig. 2]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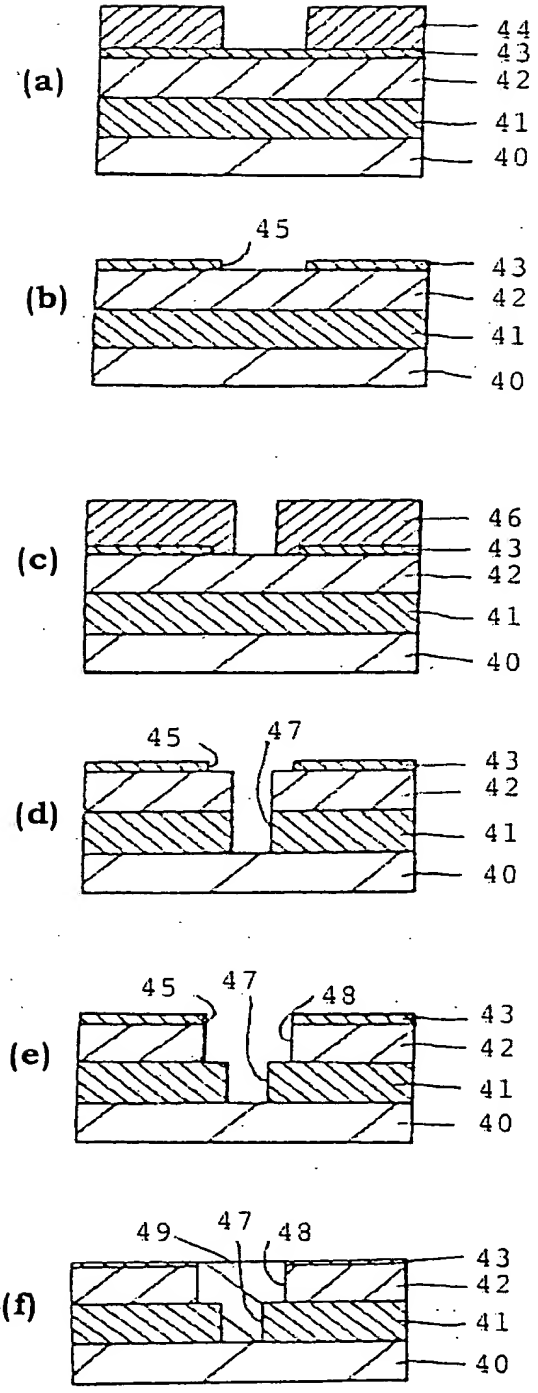
[Fig. 3]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[NAME OF THE DOCUMENT] Abstract of the Disclosure

[ABSTRACT]

[OBJECT] The object is to provide a method for producing a semiconductor device which is capable of forming a via hole and an interconnection groove without generating film thinning of an interlayer insulating film provided below a resist pattern even in the case there occurs a thinning of the resist pattern used as a mask when an organic insulating film is applied in a dual damascene process.

[EFFECT] A method for producing a semiconductor device comprising:

forming an opening by etching using resist patterns 7and 9 in a multi-layered film having a first organic insulating film 3, a first etching stop film 4 and a second organic insulating film 5 layered in this order such that the opening penetrates from the second organic insulating film 5 to the first organic insulating film 3,

wherein a second etching stop film 6 is formed between the resist patterns 7 and 9 and the second organic insulating film 5 to protect the second organic insulating film 5 from being etched during the formation of the opening.

[SELECTED FIGURE] Figure 1